SREENATH S

DESIGN VERIFICATION ENGINEER

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CAREER OBJECTIVE

My career objective is to pursue a challenging position in the field of VLSI Design and Verification, where I can leverage my knowledge of digital design, RTL coding, and verification methodologies (Verilog/System Verilog, UVM) to contribute to high-performance chip design. Eager to learn and grow in a dynamic semiconductor environment while enhancing my technical expertise and problem-solving skills. I have hands-on experience in EDA tools such as Xilinx ISE , Vivado, VCS, Questa sim.

PROFESSIONAL TRAINING

Maven Silicon Softech Pvt. Ltd. August 2024-July 2025

- Advanced VLSI Design and Verification.

EDUCATION

PROGRAM	INSTITUTE/BOARD	CGPA	YEAR
BE-Electronics and communication engineering	K Ramakrishnan College of Engineering	7.40	2025
Higher secondary Education (class XII)	The Higher Secondary School for Boys	90%	2021
Secondary Education (class X)	The Higher Secondary School for Boys	85%	2019

SKILLS SUMMARY

- **Languages:** Verilog HDL, Systemverilog, UVM.
- **Scripting Language:** PERL.
- **Protocols:** AMBA, ARM, RISC
- **Databases/OS:** Windows, Ubuntu.
- **Tools:** Tessent scan, VCS, Questa sim, Vivado, Xilinx, MATLAB.
- **Soft Skills:** Critical Thinking, Problem-Solving, Effective Communication.

PROJECTS

ROUTER 1X3 DESIGN | **Tools: VCS, Questasim**

- Developed code for individual modules like FIFO , synchronizer, controller, and register using Verilog.
- Integrated all these modules to build the complete 1x3 router system, ensuring smooth communication between each block.
- simulated the design using tools like QuestaSim and Vivado, verified functionality, and debugged any issues related to data flow, timing, or synchronization.
- Optimized the design for area and timing performance, and documented the architecture, simulation results, and final observations for reporting or presentation.

AHP TO APB BRIDGE RTL VERIFICATION | **Tools: VCS, Questasim**

- Designed an RTL bridge module in Verilog to convert AHB transactions to APB format.
- Implemented FSM-based control logic for address phase, write/read operations, and APB handshaking.
- Developed a SystemVerilog UVM testbench with directed and random testcases.

IMAGE PROCESSING APPLICATION | **Tools: Vivado, Xilinx ISE**

- Developed the architecture of the ROBA multiplier, choosing the appropriate rounding techniques for better performance.
- Implemented the logic in (HDL) like Verilog, ensuring correct operation and efficiency.
- Utilized Kogg stone adder to get the output accurately.

INTERNSHIP

EMBEDDED C | **Aug-2023**

- Completed an internship on Embedded C through Galvin technology.
- Gained hands-on experience in embedded systems programming using Embedded C.
- Developed LCD codes and implemented them on arduino board.

WORKSHOP AND PRESENTATION

EMBEDDED WORKSHOP |

- Attended an enriching workshop at IIT Madras, surrounded by a highly intellectual and inspiring environment.
- Hands-on activities and group discussions were highlights, allowing practical application of knowledge.
- Gained real-time experience on the Arduino board by doing a simple LED code.

IDEA PRESENTATION |

- Presented an idea for implementing QR codes on student ID card
- Proposed system enables instant access to user profiles, attendance tracking, and streamlined authentication processes.
- Received positive feedback for innovative thinking and potential for scalable implementation across educational and corporate environments.

CERTIFICATES

- Microsoft Azure — Microsoft
- Design and Verification Certificate — Maven Silicon
- Circuit design and spice simulation (VSD) — Udemy
- Innovative electronics workshop certificate — Lift India

ACHIEVEMENT

- Acted as a liaison between students and faculty, voicing academic and welfare concerns to department leadership.
- Organized departmental events, facilitated student engagement activities, and contributed to the development of student support initiatives.

DECLARATION

I hereby declare that the information provided above is true and correct to the best of my knowledge and belief. I take full responsibility for the accuracy of the particulars mentioned in this resume.

Place: Trichy **-Sreenath S**